AMENDMENTS TO THE SPECIFICATION

Please replace the present title with the following rewritten title:

"A METHOD, CLOCK GENERATOR MODULE AND RECEIVER MODULE FOR SYNCHRONIZING A RECEIVER MODULE"

Please amend page 1, paragraph 2 with the following:

The present invention relates to the field of telecommunications and computer technology and more particularly to a method of ~~synchronising~~synchronizing at least one receiver module, a ~~synchronisable~~ synchronizable receiver module therefor, and a clock generator module therefor.

Please amend page 1, paragraph 4 with the following:

A central clock signal of this kind is generated for example by a central clock generator module and transmitted to the receiver modules. A clock channel of a bus to which the receiver modules are connected is provided for example for the transmission. The receiver modules then operate either directly with the clock signal tapped from the bus or for example ~~synchronise~~ synchronize their own local clock generator, provided on the respective receiver module, with the central clock signal.

Please amend page 2, paragraph 1 with the following:

In a consequently redundant system, a receiver module is however supplied not only with one clock signal but with at least one second clock signal, in which case the connected receiver modules select one of the clock signals as master ~~synchronisation~~ synchronization signal for their ~~synchronisation~~ synchronization and the other clock signal(s) serve as slave ~~synchronisation~~ synchronization signals which are selected as clock signal(s) upon the failure of the master ~~synchronisation~~ synchronization signal. Ideally all the clock signals are synchronous, the slave clock signals being ~~synchronised~~ synchronized for example with the master clock signals so that the receiver modules to be ~~synchronised~~ synchronized in principle can select any one of the clock signals as their respective master ~~synchronisation~~ synchronization signal without any phase difference.

Please amend page 2, paragraph 3 with the following:

The same problems arise even if, for reasons of redundancy, network devices in a telecommunications network are ~~synchronised~~ synchronized with more than one clock signal.

Please amend page 3, paragraph 1 with the following:

Therefore the object of the invention is to provide a method and device for a precise ~~synchronisation~~ synchronization of at least one receiver module, in particular a receiver module in a telecommunications network or in a network device of a telecommunications network.

Please amend page 3, paragraph 2 with the following:

This object is achieved by a method of ~~synchronising~~synchronizing at least one receiver module, in particular a receiver module in a telecommunications network or in a network device of a telecommunications network, which has the following steps: A first clock signal and a second clock signal are sent to the at least one receiver module. In addition, at least one item of master-slave-status information about the at least one first clock signal and/or the second clock signal is sent to the at least one receiver module. Based on the item of master-slave-status information, the at least one receiver module selects the first clock signal or the second clock signal as master-~~synchronisation~~ synchronization signal for its ~~synchronisation~~synchronization.

Please amend page 3, paragraph 3 with the following:

The invention is based on the principle that the respective receiver module, which is sent at least one first clock signal and a second clock signal, and selects the at least one first clock signal or the second clock signal as master~~-synchronisation~~ synchronization signal for its ~~synchronisation~~synchronization, is sent, in addition to the clock signals, an item of master-slave-status information about the clock signals, on the basis of which information the receiver module can determine which of the clock signals is currently the master clock signal and which clock signal is the slave clock signal. The receiver module then selects the clock signal identified as master~~-synchronisation~~ synchronization signal for its~~-synchronisation~~ synchronization and thus ~~synchronises~~ synchronizes itself with the clock signal operating with a higher degree of precision.

Please amend page 4, paragraph 1 with the following:

This has a particularly advantageous effect if a plurality of receiver modules~~-synchronise~~ synchronize themselves with the same clock signal identified as master~~-synchronisation~~ synchronization signal and do not arbitrarily select one of the clock signals which possibly have phase shifts.

Please amend page 4, paragraph 2 with the following:

The invention can be used advantageously in any system with redundant clock distribution. The system can consist of one single device or for example a communications network. In a particularly preferred embodiment the invention is used in a transmission network, in particular a transmission network with a synchronous digital hierarchy (SDH) or in a network device of the transmission network, for example in a cross-connect of a SDH transmission network, a SONET network device (SONET = synchronous optical network) or a PDH network device (PDH = plesiosynchronous digital hierarchy). The receiver modules consist for example of input/output modules or switching matrix modules, which in all events require precise ~~synchronisation~~ synchronization for smooth mutual cooperation.

Please amend page 4, paragraph 5 bridging onto page 5 with the following:

The master-slave-status information can also be contained in the respective clock signals, at least partially so-to-speak as "in-band-identifier". Here different variants are conceivable. For example a master/slave identifier, for example in the form of one bit, could be attached to the clock signals. Moreover, only that clock signal to which a master identifier is added could be characterised as master~~-synchronisation~~ synchronization signal, while clock signals with no identifier are automatically regarded as slave clock signals. Additionally, only the slave clock signals, not however the master clock signal, could be identified.

Please amend page 5, paragraph 1 with the following

Advantageously, one of the clock signals is defined as a preferred master-~~synchronisation~~ synchronization signal. If it is then undetectable, on the basis of the item of master-slave-status information, as to which of the clock signals is to be selected as the master-~~synchronisation~~ synchronization signal, for example because the master-slave-status information is not sent or is sent faultily to the respective receiver module or the master-slave-status information identifies more than one clock signal as master-~~synchronisation~~ synchronization signal, the receiver module selects the clock signal defined as preferred master-~~synchronisation~~ synchronization signal. Faults relating to the master-slave-status information thus hardly affect the precision of the ~~synchronisation~~synchronization.

Please amend page 5, paragraph 3 bridging onto page 6 with the following:

The clock signals distributed by the clock generator modules are preferably synchronous with one another. For this purpose at least one first (master) clock generator module, which for example normally generates the clock signal serving as master-~~synchronisation~~ synchronization signal, sends a second (slave) clock generator module ~~a synchronisation~~ synchronization signal from which the second clock generator module can detect the correct function of the first clock

generator module. The two clock generator modules are supplied with a base clock signal, for example by the same I/O port, and thus run in synchronism.

Please amend page 6, paragraph 1 with the following:

If the second (slave) clock generator module no longer receives the ~~synchronisation~~ synchronization signal and consequently the first clock generator module no longer operates correctly, the second (slave) clock generator module becomes the (master) clock generator module and preferably the clock signal generated by the second clock generator module then becomes the master ~~synchronisation~~ synchronization signal.

Please amend page 6, paragraph 2 with the following:

In principle however it is also possible for the ~~synchronisation~~ synchronization signal sent from the first clock generator module to the second not only to comprise a pure "sign of life" but also to contain information for the ~~synchronisation~~ synchronization of the second clock generator module. For example, the clock signal generated by the first clock generator module could be sent to the second clock generator module for the ~~synchronisation~~ synchronization thereof.

Please amend page 7, paragraph 3 bridging onto page 8 with the following:

In a preferred variant, the receiver module(s) are sent at least one third clock signal with which the receiver module(s) can perform a fine ~~synchronisation~~synchronization. For example, the master-and-slave ~~synchronisation~~ synchronization signals serving for basic ~~synchronisation~~ synchronization can be transmitted at a bit rate particularly suitable for measurement purposes, for example 2 Mbit/s, while the clock signal(s) serving for the fine ~~synchronisation~~ synchronization can be transmitted at a different, higher clock frequency, for example the 2.43 MHz frequency typically used in the case of SDH, which however cannot be measured or can be measured only with difficulty when conventional measuring instruments are used.

Please amend page 8, paragraph 1 with the following:

In a particularly preferred variant of the invention it is taken into account that phase differences can occur between the clock signals received by a receiver module. These phase differences can be caused for example by ~~unsynchronised~~ unsynchronized or inadequately ~~synchronised~~ synchronized clock generator modules or by propagation time differences because the clock signals are transmitted to a respective receiver module on lines of different length. However, in the receiver module(s) there are provided delay means assigned to the clock signals, for example shift registers which can be dynamically scanned by means of multiplexers, with which the respective receiver module can correct any phase differences present between the

clock signal serving as master ~~synchronisation~~ synchronization signal and the clock signal(s) serving as slave ~~synchronisation~~ synchronization signals, so that the receiver module can at any time switch-over without a phase jump between the clock signals made available by the delay means. Here it is particularly advantageous for the receiver module to delay the first selected clock signal, for example the clock signal selected as master ~~synchronisation~~ synchronization signal, by a predetermined delay time which preferably corresponds to a maximum expected propagation time difference between the master clock signal and the slave clock signal(s). If for example the cables used for the transmission of the clock signals have a length of between 0 metres and at the maximum 200 metres, a signal propagation time on a 200 metre cable is set for example as predetermined delay time. The unselected clock signal, for example the respective slave clock signal(s), is/are likewise firstly delayed by the predetermined delay time. Then, however, the delay of the unselected clock signal is adapted so that finally all the clock signals at the outputs of the delay means are at least approximately in-phase.

Please amend page 10, paragraph 1 with the following:

A network device NWE contains receiver modules MOD1, MOD2 which are supplied with clock signals TS1, TS3 and TS2, TS4 respectively by clock generator modules GEN1, GEN2. Apart from a possible phase difference between them, the clock signals TS1, TS2 are redundant clock signals, from which the receiver modules MOD1, MOD2 select one signal as

master ~~synchronisation~~ synchronization signal for their ~~synchronisation~~synchronization. The clock signals TS3, TS4 are clock signals which are sent in addition to the clock signals TS1, TS2 and which serve for the fine ~~synchronisation~~ synchronization of the receiver modules MOD1, MOD2. In the present case the clock signals are likewise mutually redundant clock signals, from which the receiver modules MOD1, MOD2 select a clock signal TS3 or TS4.

Please amend page 11, paragraph 2 with the following:

The receiver modules MOD1, MOD2 to be ~~synchronised~~ synchronized consist for example of input/output assemblies, switching matrices or stages thereof, or other modules which must operate in synchronism for the smooth operation of the network device NWE.

Please amend page 11, paragraph 3, with the following:

From the I/O port IO1, the (external) clock signal TEX1 is transmitted via connections VG11, VG12 to the clock generator modules GEN1, GEN2, and from the I/O port IO2 the clock signal TEX2 is transmitted via connections VG21, VG22 to the clock generator modules GEN1, GEN2. The clock generator modules GEN1, GEN2 select that one of the clock signals TEX1, TEX2 which has the best clock quality. The respective clock quality is contained for example as so-called "~~synchronisation~~synchronization status message" (SSM) in SDH frames and can thus be detected by the I/O ports IO1, IO2 and/or the clock generator modules GEN1, GEN2.

According to the SDH standards of the ETSI (= European Telecommunications Standards Institute) the SSM can for example have the following meanings in descending order of quality: "primary reference clock", "transit node", "local node", "SDH equipment clock" and "do not use". With the "do not use" identifier, a SDH node operating as slave clock signals to a SDH node serving as clock source that it has currently selected its clock signal as reference and consequently a clock signal sent (back) by itself (= slave clock) to the SDH node operating as clock source cannot be used for its ~~synchronisation~~synchronization. The previously described and further ~~synchronisation~~ synchronization status messages (SSMs) for SDH- and SONET transmission networks are standardized by the ITU (International Telecommunications Union).

Please amend page 12, paragraph 1 with the following:

By means of clock generating means which have not been shown, for example with so-called phase locked loops (PLL), from the clock signals TEX1, TEX2 serving so-to-speak as basic clock signals the clock generator modules GEN1, GEN2 on the one hand generate the clock signals TS1, TS2, which in the present case are so-called frame clock signals and are transmitted at a bit rate of 2,048 megabits per second, and also generate the clock signals TS3, TS4, which are simple clock signal pulses for the fine ~~synchronisation~~ synchronization of the receiver modules MOD1, MOD2 and for example have a frequency of 2.43 Megahertz. Due to

their commonplace frequency the frame clock signals TS1, TS2 can be analyzed using known, commercially available measuring instruments.

Please amend page 12, paragraph 2, bridging onto page 13 with the following:

The frame clock signals TS1 TS2 contain a plurality of base frames which are cyclically repeated, for example with a frequency of 8 Kilohertz (kHz), and which themselves serve as clock signals. The base frames, which for example are cyclically transmitted at 8 kHz, contain quality identifiers and further ~~synchronisation~~ synchronization signals or frames, for example a 1 Hz clock signal ONEHZ. The 1 Hz clock signal ONEHZ can for example consist of one bit in the base frame which changes every 500 milliseconds between the values "0" and "1". The quality identifiers are for example individual bits or bit sequences and comprise the above explained SSM identifier sent from the I/O ports IO1, IO2 to the clock generator modules GEN1, GEN2, identifiers CUX, GENX, IDX, serving as source identifiers, and an item of master-slave-status information MSX.

Please amend page 13, paragraph 2, bridging onto page 14 with the following:

In the present case the clock generator modules GEN1, GEN2 ~~synchronise~~ synchronize one another, sending one another ~~synchronisation~~ synchronization data SY serving as ~~synchronisation~~ synchronization signals via a connection VSY. The transmitting and receiving

means required for this purpose, for example corresponding integrated circuits, have not been shown for reasons of clarity. Inter alia, the clock generator modules GEN1, GEN2 negotiate as to which of the two modules operates as master clock generator module and which as slave clock generator module. Accordingly, the clock generator modules GEN1, GEN2 set the master-slave-status information MSX in the clock signals TS1, TS2 at the values "master" or "slave", for example at logic "1" or "0". In the present arrangement, the clock generator module GEN1, GEN2 operating as master clock generator module switches itself with priority to the I/O port IO1 or IO2 selected as source for the basic clock signal TEX1, TEX2, and the clock generator module GEN1, GEN2 operating as slave clock generator module in series therewith; the converse applies in the case of a change in the master-slave status. In principle however, the clock generator modules GEN1, GEN2 could also scan in parallel the I/O port IO1, IO2 selected as source for the basic clock signal TEX1, TEX2. Moreover, in addition to the I/O ports IO1, IO2, further I/O ports, optionally serving as clock signal source, could also be provided.

Please amend page 15, paragraph 1, with the following:

As a function of that clock signal TS1 or TS2 in which the master-slave-status information MSX is set at "master", the receiver modules MOD1, MOD2 select the clock signal TS1 or the clock signal TS2 as master ~~synchronisation~~ synchronization signal and ~~synchronise~~ synchronize themselves therewith.

Please amend page 16, paragraph 1, with the following:

From the delay means D31, D11; D42, D21 the clock signals TS3, TS1; TS4; TS2 are sent to a change-over switch SEL which is a selection means for selecting a clock signal TS1, TS2. For this purpose the change-over switch SEL and/or the ports P11, P12 serving as receiving means analyze for example the master-slave-status information MSX in the clock signals TS1, TS2. In the present case the change-over switch SEL switches over not only between the clock signals TS1 or TS2 but also between the clock signals TS3, TS4 which are assigned thereto and which serve for the fine ~~synchronisation~~synchronization.

Please amend page 16, paragraph 2, with the following:

The clock signals TS1, TS21 serve to ~~synchronise~~ synchronize a multiple frame generator MUFG which, from the clock signals TS1 or TS2, generates for example a frame FR1 with a frequency of 1 Hertz and a frame FR2 with a frequency of 8 Kilohertz. The clock signals TS3, TS4 serve for the fine ~~synchronisation~~ synchronization of a local clock generator PL1, for example in the form of a so-called phase locked loop (PLL). The clock generator PL1 emits a high-frequency clock ITS, for example at 622 MHz, and additionally ~~synchronises~~ synchronizes the multiple frame generator MUFG with a ~~synchronisation~~ synchronization signal PLS. The

fine~~synchronisation~~ synchronization with the additional clock signals TS3, TS4 constitutes an advantageous development of the invention.

Please amend page 16, paragraph 3, bridging onto page 17 with the following:

Ideally, the frame clocks FR1, FR2 formed by the multiple frame generator MUFG are substantially synchronous with the respective selected clock signal TS1 or TS2. It is also possible for the frame clocks FR1, FR2 to be able to differ from the clock signals TS1, TS2 within predetermined tolerance limits. If such a tolerance limit is exceeded, the multiple frame generator MUFG automatically ~~resynchronises~~ resynchronizes itself or receives an external reset- or ~~resynchronisation~~ resynchronization command given for example by the clock generator PL1.

Please amend page 17, paragraph 2, with the following

In the present arrangement it is provided that in normal operation only one of the clock generator modules GEN1, GEN2 sends a clock signal TS1, TS2 respectively serving as master ~~synchronisation~~ synchronization signal and the other clock generator module sends only a clock signal TS1, TS2 serving as standby- or slave ~~synchronisation~~ synchronization signal. If however a fault occurs, for example due to the failure of the connection VSY or one of the clock generator modules GEN1, GEN2, the ~~synchronisation~~ synchronization data SY are no longer

correctly received by the two clock generator modules GEN1, GEN2. In this case the clock generator module(s) GEN1, GEN2, which is/are operating in fault-free fashion, so to speak automatically assume the master mode and set the master-slave-status information MSX in the clock signals TS1, TS2 at the values "master".

Please amend page 18, paragraph 1, with the following:

When, at their two respective ports P11, P12; P21, P22, the receiver modules MOD1, MOD2 receive the clock signals TS1, TS2 with an item of master-slave-status information set at "master", it can be predefined that they select the clock signal TS1 for example as master ~~synchronisation~~ synchronization signal. It is also possible for the clock signal TS2 to be selected for example as master ~~synchronisation~~ synchronization signal by the receiver modules MOD1, MOD2, even when the two clock signals TS1, TS2 are simultaneously set at "slave".

Please amend page 18, paragraph 2, with the following:

Phase differences can occur between the clock signals TS3, TS1; TS4; TS2, due for example to inadequate ~~synchronisation~~ synchronization of the clock generator modules GEN1, GEN2 and/or due to different line lengths of the connections VM31, VM11 on the one hand and the connections VM21, VM42 on the other hand. The receiver modules MOD1, MOD2 correct such phase differences by the delay means D31, D11; D42, D21 and the phase comparator DIFF.

The delay means D31, D11; D42, D21 have the form for example of shift registers whose memory cells can be dynamically scanned via multiplexers. The memory cells which are to be scanned are set by the phase comparator DIFF in accordance with the respective phase differences between the clock signals TS3, TS1; TS4; TS2 so that the change-over switch SEL can at any time switch-over, without a phase jump, between the clock signals TS3, TS1; TS4; TS2 which are available at the output end in the delay means D31, D11; D42, D21 and which are appropriately delayed for the correction of input-end phase differences.

Please amend page 19, paragraph 1, with the following:

To simplify the drawing, only the process of phase matching of the clock signals TS1, TS2 will be described in the following. The delay means D11, D21 firstly delay each of the clocks signals TS1, TS2 by a basic delay which corresponds to a maximum expected propagation time difference or phase difference between the two signals. The propagation time difference can be determined for example on the basis of a maximum line length of cables used for the connections VM11, VM21. Then the phase comparator DIFF determines the phase difference between one of the clock signals TS1, TS2, for example the clock signal TS1 not selected as master ~~synchronisation~~ synchronization signal, and the respective other clock signal TS2, TS1, for example the clock signal TS2, and in stepped fashion adapts the delay time of the delay means D21 assigned to this clock signal TS2, TS1 so that the phase difference is reduced. Here

the delay means D11, D21, which for example each contain shift registers, are scanned in stepped fashion at different memory locations which can be set by a multiplexer, the respective clock signal TS1, TS2 is determined and is reported again to the phase comparator DIFF.

Please amend page 20, paragraph 2, with the following:

Moreover further clock generator modules and/or receiver modules to be ~~synchronised~~ synchronized could also be provided in order to further increase the redundancy.

Please amend page 20, paragraph 4, with the following:

Furthermore the clock generator modules GEN1, GEN2 could also comprise clock generator means which each operate autonomously, for example oscillators, and ~~synchronise~~ synchronize one another via the connection VSY. The external clock signals TEX1, TEX2 then would not be essential.

Please amend page 21, paragraph 1, with the following:

Additionally, one of the clock generator modules GEN1, GEN2 could be predefined so-to-speak as default master clock generator module and one as slave clock generator module, the latter ~~synchronising~~synchronizing itself with the master clock generator module and, upon the

failure thereof, so-to-speak automatically becoming the master clock generator module for the network device NWE.

Please amend page 21, paragraph 2, with the following:

Combinations of clock generator modules and receiver modules could also be formed. For example, the clock generator module GEN1 and the receiver module MOD1, and likewise the clock generator module GEN2 and the receiver module MOD2, could be combined to form a combination module of this kind and for example reciprocally ~~synchronise~~ synchronize one another.

Please delete the present Abstract of the Disclosure and replace it with the following new Abstract of the Disclosure.

A method of synchronizing at least one receiver module (MOD1, MOD2), in particular a receiver module in a telecommunications network or in a network device of a telecommunications network, has the following steps: A first clock signal (TS1) and a second clock signal (TS2) are sent to the at least one receiver module (MOD1, MOD2). In addition, at least one item of master-slave-status information (MSX) about the at least one first clock signal (TS1) and/or the second clock signal (TS2) is sent to the at least one receiver module (MOD1, MOD2). Based on the item of master-slave-status information (MSX), the at least one receiver module (MOD1, MOD2) selects the first clock signal (TS1) or the second clock signal (TS2) as master synchronization signal for its synchronization.